REMARKS

Claims 1, 2, 4 through 7, 11 through 21, 23 through 26 and 29 are currently pending in the application.

This amendment is in response to the Final Rejection in the Office Action of February 27, 2006.

35 U.S.C. § 112 Claim Rejections

Claims 2, 5 through 7, 11 through 16, 20, 21, 35 and 36 are rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which Applicants regard as the invention.

Applicants have amended the claimed invention to particularly point out and distinctly claim the subject matter of the invention to comply with the provisions of 35 U.S.C. § 112. Therefore, presently amended claims 2, 5 through 7, 11 through 21, 23 through 26, and 29 are allowable under the provisions of 35 U.S.C. § 112.

35 U.S.C. § 102(b) Anticipation Rejections

Anticipation Rejection Based on Corbett et al. (U.S. Patent No. 4,992,850)

Claims 1, 4, 17 through 19, 23 through 25, and 29 through 34 were rejected under 35 U.S.C. § 102(b) as being anticipated by Corbett et al. (U.S. Patent 4,992,850).

A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference. *Verdegaal Brothers v. Union Oil Co. of California*, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). The identical invention must be shown in as complete detail as is contained in the claim. *Richardson v. Suzuki Motor Co.*, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989).

Applicants assert that the inventions of presently amended independent claims 1, 5, 17, 19, 23, and 35 are not anticipated under 35 U.S.C. § 102 by the Corrbett et al. reference because the Corbett et al. reference does not identically describe, either expressly or inherently, each and every element of the presently claimed inventions in as complete detail as is contained in the claims.

Turning to the Corbett et al. reference, described therein is a leadframe interconnect package that is tape automated bond (TAB) bonded to circuitry on the chip and which provides a circuit connection for subsequent connection for subsequent connection to a printed circuit board. The encapsulated chips will replace both the lead frame and printed circuit board in a conventional SIMM module. The Corbett et al. reference only replaces a defective semiconductor die with another semiconductor die at the same location as the defective semiconductor die, not another location.

Applicants assert that the Corbett et al. reference fails to describe, either expressly or inherently, the elements of the claimed inventions of presently amended independent claims 1, 5, 17, 19, 23, and 25 calling for "A multi-chip module system comprising . . . a substrate having a first position having, in turn, a predetermined configuration for locating a first semiconductor device thereat and having a second position having, in turn, a predetermined configuration for locating a second semiconductor device thereat on the multi-chip module system, the second position having no semiconductor device located thereat until a semiconductor device is installed to replace a defective semiconductor device at the second position; a first semiconductor device located in the first position of the substrate for use in the multi-chip module system, the first semiconductor device having a first predetermined performance characteristic, said first semiconductor device having been burned in at said first position on said substrate; and a second known-good-die located at the second position, the second semiconductor device having a second predetermined performance characteristic.", "A multi-chip module system comprising . . . a substrate having a first position having, in turn, a predetermined configuration for locating a first semiconductor device thereat, having a second position having, in turn, a predetermined configuration for locating a second semiconductor device thereat, and having a third position having, in turn, a predetermined configuration for locating a third semiconductor device thereat on the multi-chip module system, the third position having no semiconductor device located thereat until a semiconductor device is installed to replace a defective semiconductor device at another position; the first semiconductor device located in the first position of the substrate for use in the multi-chip module system, the first semiconductor device having a first predetermined performance characteristic; and a second known-good-die semiconductor device located in the

second position of the substrate for use in the multi-chip module system, the second semiconductor device having a second predetermined performance characteristic, said first and second semiconductor devices have been burned in at said first and second positions, respectively, on said substrate.", "A multi-chip module system comprising . . . a substrate having two opposing sides, said substrate having a first position having, in turn, a predetermined configuration for locating a first semiconductor device thereat, having a second position having, in turn, a predetermined configuration for locating a second semiconductor device thereat, having a third position having, in turn, a predetermined configuration for locating a third semiconductor device thereat, the third position having no semiconductor device located thereat until a semiconductor device is installed to replace a defective semiconductor device at another position, and having a fourth position having, in turn, a predetermined configuration for locating a fourth semiconductor device thereat on the multi-chip module system, the fourth position having no semiconductor device located thereat until a semiconductor device is installed to replace a defective semiconductor device at another position; the first semiconductor device located in the first position of the substrate for use in the multi-chip module system, the first semiconductor device having a first predetermined performance characteristic; and a second known-good-die semiconductor device located in the second position of the substrate for use in the multi-chip module system, the second semiconductor device having a second predetermined performance characteristic, said first device being burned in at said first position on said substrate.", "A multi-chip module system comprising . . . a substrate having a first predetermined configuration position for locating a first semiconductor device thereat and having a second predetermined configuration position for locating a second semiconductor device thereat on the multi-chip module system, the second position having no semiconductor device located thereat until a semiconductor device is installed to replace a defective semiconductor device at another position; the first semiconductor device located in the first predetermined configuration position of the substrate for use in the multi-chip module system, the first semiconductor device having a first predetermined performance characteristic, said first semiconductor device being burned in at said first predetermined configuration position on said substrate; and a second known-good-die located at the second predetermined configuration position.", "A multi-chip module system

comprising . . . a substrate having a first predetermined configuration position for locating a first semiconductor device thereat, having a second predetermined configuration position for locating a second semiconductor device thereat, and having a third predetermined configuration position for locating a third semiconductor device thereat on the multi-chip module system, the third position having no semiconductor device located thereat until a semiconductor device is installed to replace a defective semiconductor device at another position; the first semiconductor device located in the first predetermined configuration position of the substrate for use in the multi-chip module system, the first semiconductor device having a first predetermined performance characteristic; and a known-good-die second semiconductor device located in the second predetermined configuration position of the substrate for use in the multi-chip module system, the second semiconductor device having a second predetermined performance characteristic.", and "A multi-chip module system comprising . . . a substrate having two opposing sides, said substrate having a first predetermined configuration position for locating a first semiconductor device thereat, having a second predetermined configuration position for locating a second semiconductor device thereat, having a third predetermined configuration position for locating a third semiconductor device thereat, the third predetermined configuration position having no semiconductor device located thereat until a semiconductor device is installed to replace a defective semiconductor device at another position, and having a fourth predetermined configuration for locating a fourth semiconductor device thereat on the multi-chip module system, the fourth predetermined configuration position having no semiconductor device located thereat until a semiconductor device is installed to replace a defective semiconductor device at another position; the first semiconductor device located in the first predetermined configuration position of the substrate for use in the multi-chip module system, the first semiconductor device having a first predetermined performance characteristic; and a known-good-die second semiconductor device located in the second predetermined configuration position of the substrate for use in the multi-chip module system, the second semiconductor device having a second predetermined performance characteristic." In contrast to the elements of the presently claimed inventions of presently amended independent claims 1, 5, 17, 19, 23, and 25, Applicants assert that the Corbett et al. reference is absent any description of a second

position, a third position, and a fourth position for a semiconductor device to be placed thereat. The Corbett et al. reference only describes placing a semiconductor die at the same position that a defective semiconductor device has been removed therefrom. The presently claimed inventions of presently amended claims 1, 5, 17, 19, 23, and 35 are not described whatsoever by the Corbett et al. reference, either expressly or inherently, as Corbett et al. only replace defective semiconductor die with another semiconductor die at the same location as the defective semiconductor die was located, not replacing a defective die at a vacant location as in the claimed inventions. Such is not the claimed inventions of presently amended independent claims 1, 5, 17, 19, 23, and 35. Therefore, Applicants assert that presently amended independent claims 1, 5, 17, 19, 23, and 35 are allowable as well as the currently pending dependent claims therefrom.

In summary for the reasons set forth herein, Applicants submit that claims 1, 2, 4 through 7, 11 through 21, 23 through 25, and 29 through 36 are clearly allowable over the cited prior art.

Applicants request the allowance of claims 1, 2, 4 through 7, 11 through 21, 23 through 25, and 29 through 36 and the case passed for issue.

Applicants request entry of this amendment for the following reasons:

The amendment is timely filed.

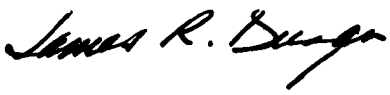
The amendment places the application in condition for allowance.

The amendment does not require any further search.

In summary, for the reasons set forth herein, Applicants assert that claims 1, 2, 4 through 7, 11 through 21, 23 through 25, and 29 through 36 are clearly allowable over the cited prior art.

Applicants request the entry of this amendment, the allowance of claims 1, 2, 4 through 7, 11 through 21, 23 through 25, and 29 through 36, and the case passed for issue.

Respectfully submitted,



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